REMARKS

Claims 1-12 and 19-32 are pending in the present application. Claims 1, 6 and 9 have been amended. Claims 19-32 have been presented herewith, and should be interpreted as reading on elected Species I. Claims 4, 5 and 7-12 have been withdrawn. Claims 13-18 have been canceled. Applicants respectfully reserve the right to file a divisional application including canceled claims 13-18.

Priority Under 35 U.S.C. 119

Applicants note the Examiner's acknowledgment of the Claim for Priority under 35 U.S.C. 119, and receipt of the certified copy of the Priority Document.

Claim Rejections-35 U.S.C. 102

Claims 1-3 and 6 have been rejected under 35 U.S.C. 102(e) as being anticipated by the Farnworth et al. reference (U.S. Patent Application Publication No. 2004/0113283). This rejection, insofar as it may pertain to the presently pending claims, is traversed for the following reasons.

The method of fabricating a semiconductor device of claim 1 includes in combination providing a semiconductor wafer...; "forming a sealing resin on the first surface of the semiconductor wafer"; "forming a plurality of external terminals on the first surface of the semiconductor wafer, wherein the external terminals respectively

electrically connect to the circuit elements and project from the sealing resin"; "forming a heat spreading material on the second surface of the semiconductor wafer, after said forming the sealing resin; and "separating the semiconductor wafer at the scribe lines after the heat spreading material is formed on the second surface of the semiconductor wafer". Applicants respectfully submit that the Farnworth et al. reference as relied upon by the Examiner does not disclose these features.

The Examiner has relied upon paragraph [0220] through paragraph [0229] and Figs. 13A – 13G of the Farnworth et al. reference as disclosing the features of claims 1-3 and 6. The Examiner has apparently interpreted the "exposed half" of back side 22E of substrate 14E, as exposed through slots 86E of etch mask 84E, as the heat spreading material of claim 1. However, corresponding slots 86E in etch mask 84E are formed in a step as described in paragraph [0222] of the Farnworth et al. reference, with respect to Fig. 13B. The formation of circuit side polymer layer 36E (interpreted by the Examiner as the sealing resin of claim 1) occurs subsequent to formation of the "exposed half" of back side 22E of substrate 14E, as described in paragraphs [0023 – 0024] with reference to Fig. 13C. Accordingly, as may be readily understood, the "exposed half" of back side 22E of substrate 14E, as exposed through slots 86E of etch mask 84E, must necessarily be formed prior to formation of circuit side polymer layer 36E (interpreted as the sealing resin).

The Farnworth et al. reference as specifically relied upon by the Examiner thus fails to disclose a method of fabricating a semiconductor device including in

combination "forming a heat spreading material on the second surface of the semiconductor wafer, after said forming the sealing resin", as would be necessary to meet the features of claim 1. Applicants emphasize that since the heat spreading material is formed after the sealing resin, contamination of the circuit elements by the heat spreading material can be avoided. In contrast, etch mask 84E of the Farnworth et al. reference is formed on back side 22E as shown in Fig. 13B, before circuit side polymer layer 36E is formed. It should also be understood that etch mask 84E is described as a silicon nitride film formed as a passivation layer. Typically, an etch mask 84E such as a silicon nitride film is not a source of contamination. Accordingly, there would be no reason to form etch mask 84E after formation of circuit side polymer layer 36E in the Farnworth et al. reference.

Applicants therefore respectfully submit that the method of fabricating a semiconductor device of claim 1 distinguishes over the Farnworth et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claims 1-3, is improper for at least these reasons.

Claim 3, as dependent upon claim 1, further features "forming a heat conductor on the second surface of the semiconductor wafer, before said forming the heat spreading material". Applicants respectfully submit that the Farnworth et al. reference as relied upon by the Examiner does not disclose these features.

As noted above, the Examiner has apparently interpreted the "exposed half" of back side 22E of substrate 14E in Fig. 13B of the Farnworth et al. reference as the heat

spreading material of claim 1. The Examiner has apparently further interpreted etch mask 84E as the heat conductor of claim 3. Applicants respectfully submit that this interpretation is improper for the following reasons.

Particularly, claim 3 features formation of a heat conductor and a heat spreading material on a semiconductor wafer. In contrast, the back side 22E of substrate 14E (semiconductor wafer) in Fig. 13B of the Farnworth et al. reference, merely includes etch mask 84E thereon. Backside 22E of substrate 14E does not have both a heat spreading **material** and a heat conductor **formed** thereon. Applicants therefore respectfully submit that the method of claim 3 distinguishes over the Farnworth et al. reference as relied upon by the Examiner, and that this rejection of claim 3 is improper for at least these additional reasons.

The method of fabricating a semiconductor device of claim 6 includes in combination "selectively forming a heat spreading material on the second surface of the semiconductor wafer, after said forming the sealing resin, wherein the scribed lines are exposed from the heat spreading material". Applicants respectfully submit that the Farnworth et al. reference as relied upon by the Examiner does not disclose forming a heat spreading material after forming a sealing resin, as would be necessary to meet the features of claim 6. Applicants therefore respectfully submit that the method of fabricating a semiconductor device of claim 6 distinguishes over the Farnworth et al. reference as relied upon by the Examiner, and that this rejection, insofar as it may pertain to claim 6, is improper for at least these reasons.

Claims 4, 5 and 7-12

Since generic claims 1 and 6 distinguish over the relied upon prior art and thus should be allowable for at least the above reasons, the Examiner is respectfully requested to rejoin and examine withdrawn dependent claims 4, 5 and 7-12, which should be allowable at least by virtue of dependency upon claims 1 and 6 respectively.

Claims 19-32

Applicants respectfully submit that claims 19-23 as dependent upon claim 1, and claims 24-28 as dependent upon claim 6, distinguish over and would not have been obvious in view of the relied upon prior art for at least the same reasons as set forth above with respect to claims 1 and 6, and by further reason of the features therein.

The method of fabricating a semiconductor device of claim 29 includes in combination providing a semiconductor wafer...; "forming a sealing resin on the first surface of the semiconductor wafer"; "forming a plurality of external terminals..."; "forming a material film that covers the second surface of the semiconductor wafer, the material film having a heat radiating ratio that is greater than a heat radiating ratio of the semiconductor wafer"; and "separating the semiconductor wafer at described lines after the heat spreading material is formed on the second surface of the semiconductor wafer".

Applicants respectfully submit that Figs. 13A – 13G of the Farnworth et al. reference as relied upon by the Examiner does not include **a material film** that covers

surface 22E of semiconductor substrate 14E, whereby **the material film** has a heat radiating ratio that is greater than a heat radiating ratio of semiconductor substrate 14E. Particularly, the only material layer or film formed on surface 22E in Fig. 13B of the Farnworth et al. reference is silicon nitride etch mask 84E. Etch mask 84E is not described or even remotely suggested as having a heat radiating ratio that would meet the features of claim 29. Applicants therefore respectfully submit that claims 29-32 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

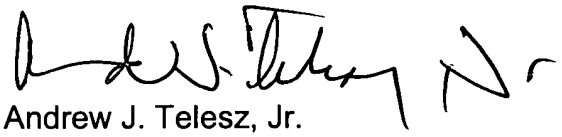
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720 in the Washington, D.C. area, to discuss these matters.

Pursuant to the provisions of 37 C.F.R. 1.17 and 1.136(a), the Applicants hereby petition for an extension of two (2) months to August 7, 2005, for the period in which to file a response to the outstanding Office Action. The required fee of $450.00 should be charged to Deposit Account No. 50-0238.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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